

Application Note

*Scaling and Cropping
with Rockwell Video Decoders*

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Scaling and Cropping with Rockwell Video Decoders

Introduction

The operations of scaling and cropping images are implemented within the same circuitry as the Ultralock™ process. Therefore, to understand how scaling operates, a description of Ultralock™ is necessary. Also, scaling and Ultralock™ are triggered by horizontal sync detection. Therefore, an explanation of how our clamping, sync detection and AGC processes operate is required.

This application note will provide a description of the clamping, sync detection and AGC processes for our older decoder products, as well as for our later decoder products. This will be followed by a description of Ultralock™, horizontal scaling/cropping, and vertical scaling/cropping. How these processes affect the operation of the output interface will conclude this application note.

Anti-Aliasing Filtering

Since digitizing aliases frequencies above half the sampling frequency, the analog video needs to be band-limited before it's digitized. The analog video input must be band-limited to 14.32 MHz in NTSC and 17.73 MHz in PAL/SECAM mode. Normal video signals do not require additional external filtering. However, if noise or other signal content is expected above these frequencies, then an anti-aliasing filter should be included in the input signal path.

Because Rockwell decoders sample at CLKx2 (8xFsc—over twice the normal rate), no external filtering is normally required at the input to the A/Ds. The Anti-aliasing filtering below these frequencies is integrated into the design of the decoder. After A/D conversion, the samples are digitally low-pass filtered and then decimated to CLKx1. The digital low-pass filter provides both the decimation filter and anti-aliasing filter functions. The digital filter reduces the video bandwidth to 6 MHz.

Some models of our decoders (82x and later) will perform additional filtering when the part is programmed to scale down greater than 2:1. Programming the LDEC bit in the Miscellaneous Control Register and HFILT bits in the SC Loop Control Register can enable these filters. This feature contains an auto-format option that changes the HFILT bits automatically depending on the value of HSCALE.

Clamping, Sync Detection and AGC

The method used to perform the AGC is the same for the newer and older versions of our decoders. Listed below are the products that have the old method, and products that have the new method.

Old Method Bt81x, Bt81xA, Bt82x, Bt848

New Method Bt82xA, Bt82xB, Bt835, Bt84xA, Bt878/9 and future products

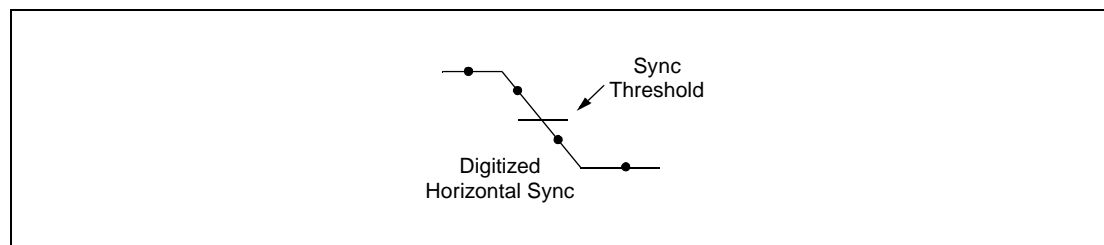
Older Decoders

The sync lock process is serial, requiring clamping, and AGC'ing, prior to horizontal and vertical lock.

Clamping

On older decoders, clamping and sync detection were performed using the combination of the SYNC_DET pin and the outputs of the A/D conversion. The SYNC_DET pin contains an analog sync detection function that is used to perform clamping and initial coarse lock. This pin detects when the signal drops below $\frac{1}{2}$ the sync height, waits a period of time (about equal to $\frac{1}{2}$ the hsync low time) and then performs a clamp operation for a short period in which the sync tip is restored to ground (see Figure 1). For signals with significant DC offset from the previous signal (for switching applications), the clamping operation may take several fields before the sync tip is clamped fully to ground. In cases where quick capture is desired after switching multiplexed inputs, the sync lock process can be accelerated by pre-clamping all inputs to identical levels.

Figure 1. Sync Threshold



AGC Operation

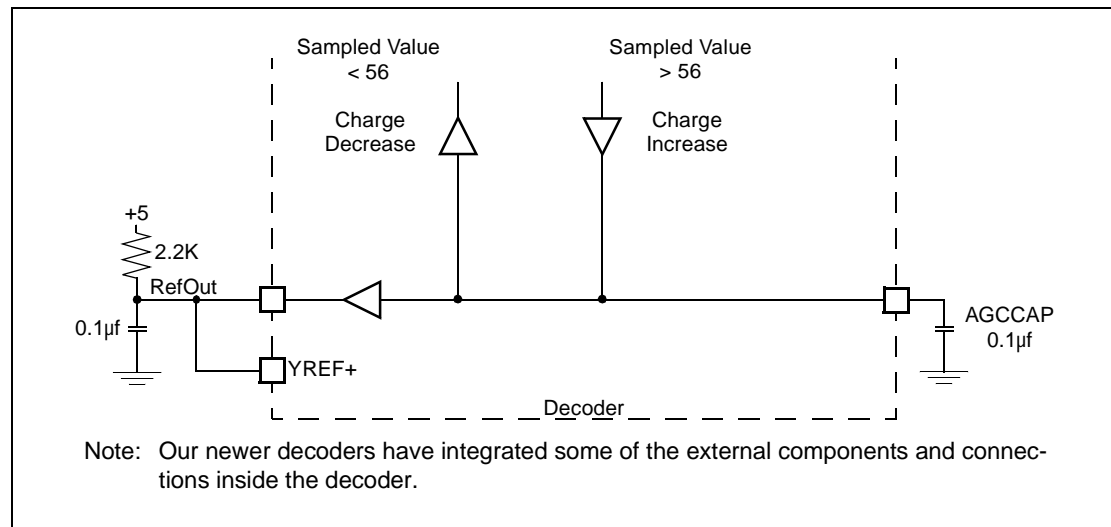
The AGC operation is depicted in Figure 2. Simply, the AGC adjusts the REFOUT voltage (which connects to the ADC ladders) until the back porch (blanking level) is equal to 56 decimal. The sampling location is determined by the value programmed in the AGC_DELAY register. This process occurs for every line.

The analog input signal is converted to digital, using the ADC, then digitally low pass filtered to remove the color burst from the back porch. A sample is taken (as programmed in the AGC_DELAY register) and compared against the desired value of 56. If the sample is too low, then charge is removed from the AGCCAP and the voltage at REFOUT is lowered. Lowering REFOUT

will then cause that same voltage to appear higher in the converted data. If the sample is too high, then charge is added to the AGCCAP and the voltage at REFOUT is increased.

The AGC algorithm is configured so that only a small amount of charge is added or removed each line. Therefore, it may take a number of fields before the AGC is equalized after connecting or switching signals.

Figure 2. AGC Circuit and Required External Components



Sync Detection

Now that the signal is clamped and AGC'd properly, the digital sync detector is used to precisely determine the time when the falling edge of horizontal sync occurred.

HRESET

After the AGC equalizes the signal, the horizontal sync will be detected if the digital value drops below $\frac{1}{2}$ the sync height (digital value of 28 decimal). This event triggers the generation of an HRESET pulse that is 64 CLKx1 periods long. Note that, although this identifies the location of horizontal sync, HRESET will occur at the expected location of that horizontal sync. The difference between the actual and expected locations of the horizontal sync is used for error correction to adjust the expected location of the horizontal sync for the next line. For more detailed insight to this circuit, see Application Note AN40_1A, Sync Locking in Source Multiplexing Applications.

VRESET

Vertical sync detection is performed at the end of the serration pulses. An algorithm detects a vertical sync by searching for a proper sequence of zero and non-zero levels. This triggers the generation of VRESET which is typically 6 lines long (it may be shorter for time-varying sources such as VCRs).

Newer Decoders

The differences between the older and newer decoders are:

1. There is no longer a need for an analog sync detect circuit. All detection is now performed in the digital domain. Some of the decoders (82xA series) still have the SYNC_DET on the chip for compatibility with designs which may have used previous versions of the chip. New designs should tie this pin, if present, to VAA.
2. The location of the horizontal sync is now digitally identified for clamping and AGC purposes.

Detection requires approximately the same time to acquire as the older method. AGC is otherwise unchanged.

Ultralock™ Operation

The Ultralock™ algorithm permits the use of an independent asynchronous clock to perform sampling. This provides much better video quality than a PLL-based approach since the decoding clock for the color subcarrier is fixed. The processes of line length correction, clock synchronizing, scaling and cropping are essentially performed in a single operation, but will be described here as more of a serial process.

Principles

UltraLock™ is based on sampling using a fixed-frequency stable clock. Since the video line length can vary (particularly for sources such as VCRs), the number of samples generated per line using a fixed-frequency sample clock will also vary. If the number of generated samples per line is always greater than the number of pixels per line required by the particular video format, the number of acquired samples can be reduced to fit the required number of pixels per line. This is achieved using an interpolation algorithm.

Our decoders (except Bt812) require an $8 \times F_{sc}$ ($8 \times$ Color Subcarrier Frequency, 28.64 MHz for NTSC and 35.47 MHz for PAL) crystal or oscillator input signal source. The $8 \times F_{sc}$ clock signal, or CLKx2, is divided down to CLKx1 internally (14.32 MHz for NTSC and 17.73 MHz for PAL). Both CLKx2 and CLKx1 are made available to the system. UltraLock™ uses CLKx1 for its processing. The ADC data, sampled at the CLKx2 rate, is low pass filtered and then decimated to create samples at the CLKx1 rate.

At a $4 \times F_{sc}$ (CLKx1) sample rate there are 910 samples for NTSC and 1,135 samples for PAL/SECAM within a nominal line time interval (63.5 ms for NTSC and 64 ms for PAL/SECAM). For square pixel NTSC and PAL/SECAM formats there are only 780 and 944 pixels per video line, respectively. This is because the square pixel clock rates are slower than a $4 \times F_{sc}$ clock rate: for example, 12.27 MHz for NTSC and 14.75 MHz for PAL.

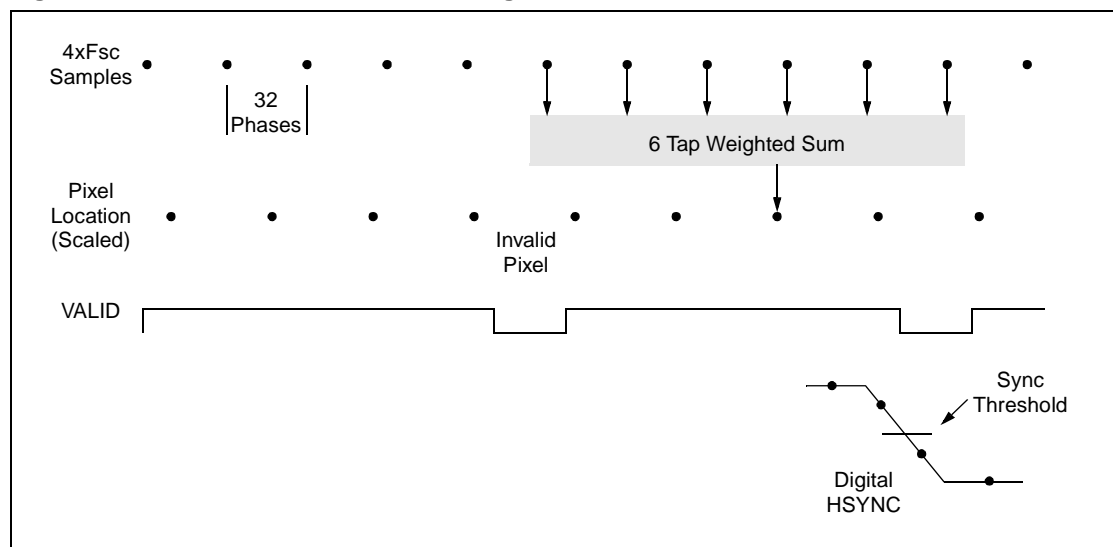
UltraLock™ is used to extract any programmable number of pixels from the original video stream. One restriction is that the number of samples in a line must be greater than the number of active pixels desired for that line.

The internal timing generator limits the number of samples in a line to the range of 7/8 to 9/8 of the nominal number of samples in a line. Therefore, the maximum number of pixels that can be extracted per line is $7/8 * 910 = 796$ for NTSC or $7/8 * 1135 = 993$ for PAL.

Horizontal Scaling and Cropping

The generalized horizontal scaling and Ultralock™ algorithm is depicted in Figure 3. The precise location of the falling edge of horizontal sync is located between two samples by interpolating between these samples.

Figure 3. Ultralock and Horizontal Scaling



Horizontal Interpolation

Interpolation means to insert new data between or among others. This means that the output data has only an indirect relationship to the information sampled. In this case, depending on the scaled value, the data output may relate to the exact pixel sampled, or, due to fractional scaled values, the output pixel may (and usually will) land in between the sampled values. In that event, the interpolation filter determines the value that would have been there, had our sample clock been scaled instead.

The interpolation algorithm compares the 4xFsc samples and the desired, scaled sample period. The desired scaled sample period and offset is determined by the following:

1. Scaling value, as programmed into the HSCALE register;
2. The inter-sample sync location.

The algorithm uses polyphase interpolation to generate the scaled pixels from the 4xFsc sampled pixels. The desired sampled pixel location is determined to within 1/32 of a 4xFsc-sample period (the Bt835 has 1/64th resolution for luma). These values, between 1 and 32, are used to determine the coefficients used by the 6-tap weighted sum interpolator to calculate the output pixel luminance value.

Horizontal Scaling and Cropping

For chroma data, the same 1 of 32 samples are used, but fewer coefficients are used by a 2-tap interpolator.

Invalid Pixels

Because there are more samples at the $4 \times F_{sc}$ sample rate than at the desired scaled output pixel rate, there are times when there are two $4 \times F_{sc}$ samples within the period of one desired scaled output rate pixel. Our output interface is based on the $4 \times F_{sc}$ sample clock, so there is a $4 \times F_{sc}$ clock period without any correlating valid scaled pixel data to be output. This clock period must be ignored, since it is an invalid pixel. No pixels are “dropped.”

There are more clock periods per line than valid pixels to be output, so some clock periods will not carry any valid pixel data. Think of this as invalid clock periods, with the data lines still wiggling without direction, producing invalid pixels. These are gated out with DVALID, often through QCLK.

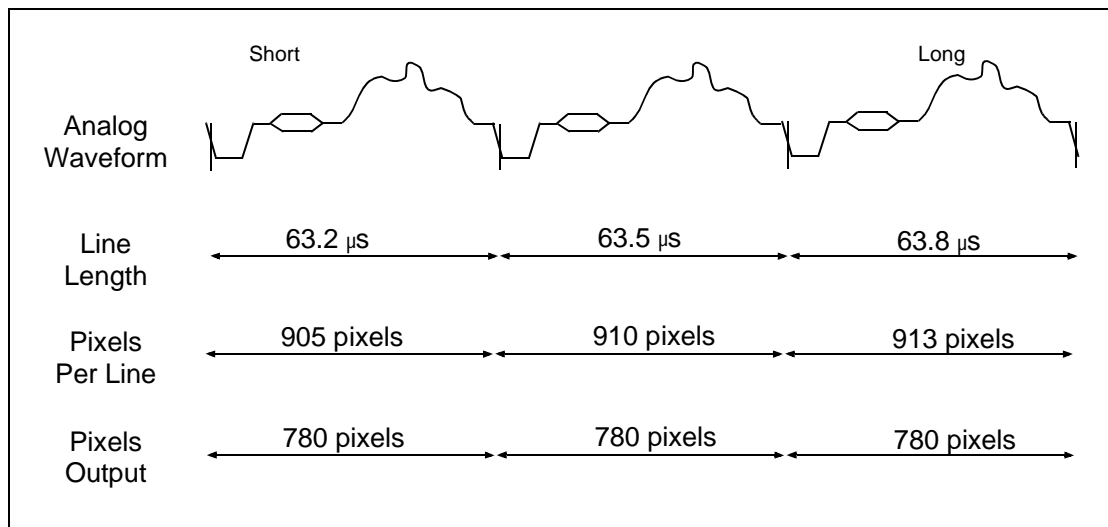
Line Length

UltraLock™ accommodates line length variations, from nominal, in the incoming video by always acquiring more samples (at an effective $4 \times F_{sc}$ rate) than are required by the particular video format. UltraLock™ interpolates the required number of pixels so that it maintains the stability of the original image, despite variation in the line length of the incoming analog waveform. It then outputs the correct number of pixels per line.

The decoder implements this by always counting the number of pixels per line. Based on the pixel count of the previous line, the period of the desired pixels is adjusted to maintain the scaling required. The decoder assumes that the pixel count change from one line to the next is small.

The example illustrated in Figure 4 shows three successive lines of video being decoded for square pixel NTSC output. The first line is shorter than the nominal NTSC line time of $63.55 \mu s$. On this first line, a line time of $63.2 \mu s$ is sampled at $4 \times F_{sc}$ (14.32 MHz) and generates only 905 samples. The second line matches the nominal line time of $63.55 \mu s$ and provides the expected 910 samples. Finally, the third line is too long at $63.8 \mu s$ and 913 samples are generated. In all three cases, UltraLock™ outputs only 780 pixels.

For instantaneous variations, or when variations are severe (greater than $\pm 1/8$ of nominal line length), such as with VCRs or noisy tuner signals, images may not properly align with previous lines. A short line would continue to output data from the next line, and a long line would truncate, with remnants wrapping to the next line, which could, potentially, look like a short line. Hence, the “wiggly” image, as the decoder attempts to capture very unstable video. Lines which are too short, but only marginally under the $-1/8$ or nominal line limit may be recovered by implementing the HACTIVE_extend bit, on those decoders so equipped. This register bit will allow the horizontal active region to extend beyond the beginning of HRESET, and thereby increases the number of samples available. This can be useful for controllers intolerant of short lines, such as those counting pixels.

Figure 4. Ultralock Behavior for NTSC Square Pixel Output

Horizontal Cropping

Horizontal cropping is relatively independent of the scaling and interpolation operations. Scaling is controlled by the HSCALE parameter. The HDELAY and HACTIVE registers control cropping.

The HDELAY register is used to determine the number of scaled pixels, not $4 \times F_{sc}$ clocks ($CLK \times 1$), from the falling edge of hsync to the start of active video. The image can be horizontally cropped on the left side by using a value of HDELAY greater than the nominal value for the scaled image. Care must be taken when increasing the HDELAY value so that $HDELAY + HACTIVE$ does not exceed the total number of desired scaled pixels per line. The image can be cropped on the right side by adjusting the HACTIVE register to a smaller value.

Horizontal Scaling Registers

The following example illustrates the use of scaling and cropping features with NTSC square pixel format. This example applies equally well to other video standards when the appropriate numbers are used.

Full resolution NTSC square pixel format requires 780 pixels per line (Table 1). However, the decoder produces 910 samples, nominally, per line of video. The Rockwell decoder scales every pixel—including those in the synchronization and blanking intervals—by a factor of $780 / 910 = 0.8571429$. That is, for full resolution NTSC square pixel format, the decoder generates 0.8571429 pixels per clock cycle, interpolating to achieve the final pixel count.

First, the number of active pixels for the Horizontal Active (HACTIVE) period that needs to be output must be determined. Then the scale factor (HSCALE) needs to be determined. Finally, the number of scaled pixels that need to be allocated for the Horizontal Delay (HDELAY) period, or the time before active video is output, needs to be determined. In this example, the total number of scaled pixels for the Horizontal Delay period and the Horizontal Active period must be less than 780. There are a few pixels after the end of the active period and before the start of the next line (front porch).

Horizontal Scaling and Cropping

To determine the proper values for the HDELAY and HACTIVE registers, you can equate everything to the value of one CLKx1 cycle, which is 69.84167 ns (NTSC). The interval between horizontal sync and valid video data is 9.4 μ s (minimum) for NTSC. This means that $9.4 \mu\text{s} / 69.84167\text{ns} = 135 \text{ CLKx1}$ cycles of delay is required before valid video data exists. The interval for valid video data is 52.66 μ s for NTSC. This means that $52.66 \mu\text{s} / 69.84167\text{ns} = 754 \text{ CLKx1}$ cycles are required to capture all the valid video data. The period after valid video data and the horizontal sync, or the front porch, is 1.49 μ s for NTSC. In other words, $1.49\text{ns} / 69.84167\text{ns} = 21 \text{ CLKx1}$ cycles are required to capture the remaining pixels after valid video data. The total result for NTSC is $63.55 / 69.24167\text{ns} = 910$ ($135 + 754 + 21 = 910$) CLKx1 periods.

Figure 5 illustrates calculating samples for NTSC.

Figure 5. Calculating Samples for NTSC

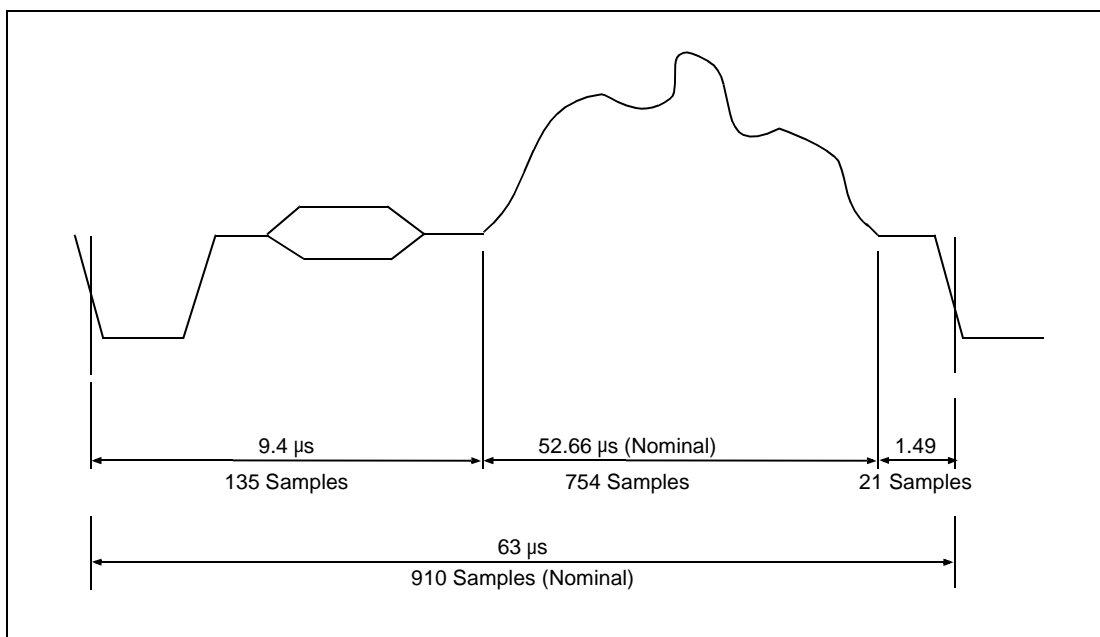


Table 1. Scaling Ratios for Popular Formats Using Frequency Values

Scaling Ratio	Format	Total Resolution (including sync and blanking interval)	Output Resolution (Active Pixels)	HSCALE Register Values	VSCALE Register Values	
					Both Fields	Single Field
Full Resolution 1:1	NTSC SQ Pixel	780x525	640x480	0x02AA	0x0000	N/A
	NTSC CCIR601	858x525	720x480	0x00F8	0x0000	N/A
	PAL CCIR601	864x625	720x576	0x0504	0x0000	N/A
	PAL SQ Pixel	944x625	768x576	0x033C	0x0000	N/A
CIF 2:1	NTSC SQ Pixel	390x262	320x240	0x1555	0x1E00	0x0000
	NTSC CCIR601	429x262	360x240	0x11F0	0x1E00	0x0000
	PAL CCIR601	432x312	360x288	0x1A09	0x1E00	0x0000
	PAL SQ Pixel	472x312	384x288	0x1679	0x1E00	0x0000
QCIF 4:1	NTSC SQ Pixel	195x131	160x120	0x3AAA	0x1A00	0x1E00
	NTSC CCIR601	214x131	180x120	0x3409	0x1A00	0x1E00
	PAL CCIR601	216x156	180x144	0x4412	0x1A00	0x1E00
	PAL SQ Pixel	236x156	192x144	0x3CF2	0x1A00	0x1E00
ICON 8:1	NTSC SQ Pixel	97x65	80x60	0x861A	0x1200	0x1A00
	NTSC CCIR601	107x65	90x60	0x7813	0x1200	0x1A00
	PAL CCIR601	108x78	90x72	0x9825	0x1200	0x1A00
	PAL SQ Pixel	118x78	96x72	0x89E5	0x1200	0x1A00
Notes: 1. PAL-M HSCALE and VSCALE register values should be the same as for NTSC. 2. PAL-N combination-HSCALE register values should be the same as for CCIR resolution NTSC. VSCALE register values should be the same as for CCIR resolution PAL. 3. SECAM-HSCALE and VSCALE register values should be the same as for PAL.						

To summarize, the following periods are required:

- 135 CLKx1 periods are required for Horizontal Delay (HDELAY).
- 754 CLKx1 periods are required for Horizontal Active (HACTIVE).
- 21 CLKx1 periods are required for the front porch.

The HDELAY and HACTIVE registers must be specified in scaled pixels, and not in CLKx1 cycles. The 780/910 scaling ratio for square pixel NTSC is the key to calculating the correct number of scaled pixels. Because 0.8571429 pixels are generated per clock pulse (in this example), the following formula may be used to calculate the number of scaled pixels required:

HDELAY: (HDELAY in CLKx1 periods * scaling ratio =) $135 * 0.8571429 = 116$ scaled pixels (must be even)

HACTIVE: (HACTIVE in CLKx1 periods * scaling ratio =) $754 * 0.8571429 = 646$ scaled pixels

Front porch: (F.P. in CLKx1 periods * scaling ratio =) $21 * 0.8571429 = 18$ scaled pixels

These are exact calculations for a 780/910 ratio of pixels to CLKx1 cycles. However, the HACTIVE value equates to 646 scaled pixels where a standard number of active pixels, 640, is typically used. The extra six pixels would be added as part of the front porch. The video is actually

Horizontal Scaling and Cropping

cropped by six scaled pixels at the end of each active horizontal line. Alternatively, you may change the HDELAY register to 122 scaled pixels. In this case, the video is cropped by six scaled pixels at the beginning of each horizontal line.

For a single image size, this method works fine. However, for arbitrary scaling, as in a drag and stretch window application, this results in the image re-centering with each re-scale calculation, due to the six pixel error correction always weighted on the same side of the image.

Rockwell provides an additional approach to reconcile the number of scaled pixels. For the default configuration, the HDELAY register is set to 120 scaled pixels, while the HACTIVE is set to 640 scaled pixels. The video is cropped by four scaled pixels at the beginning of each horizontal line and is cropped by two scaled pixels at the end of each horizontal line. This more closely keeps the image centered in the window, keeping in mind that pixels must be in even Y/C pairs. This is the reason the pixels cannot be split 3/3, i.e., the Y/C byte order sequence would be lost.

This is the standard approach. Most of our decoders support exact 3/3 splitting of cropped pixels, through the use of a manually programmed CBSense bit, which restores inverted CrCb ordering to accommodate odd values of HDELAY.

HACTIVE

This register is simply programmed with the desired number of active pixels per line.

HSCALE

Assuming that the active region is known, the next step is to determine the HSCALE value. This is based on HACTIVE, or calculated based on knowing the total number of pixels per line. The value for the HSCALE register can be calculated using the formula in Figure 6:

Figure 6. Generic HSCALE Formula

$$\text{HSCALE} = [(1 / \text{Scaling_Ratio}) - 1] * 4096$$

For example, to achieve horizontal image scaling for square pixel NTSC, use the formula in Figure 7 and replace (Pdesired) with the exact number of total pixels required. For 2:1 scaling, for example, Pdesired pixels would be replaced with 455 pixels (910/2). For NTSC square pixels (780x525), 2:1 scaling (CIF) uses 390 pixels (780/2).

Figure 7. Total Line Pixels Formula

$$\begin{aligned} \text{NTSC: HSCALE} &= [(910 / \text{Pdesired}) - 1] * 4096 \\ \text{PAL/SECAM: HSCALE} &= [(1135 / \text{Pdesired}) - 1] * 4096 \end{aligned}$$

where Pdesired equals the total number of desired scaled pixels per line (including active, sync, and blanking).

The value for the HSCALE register can also be calculated using an “ideal” number of active pixels, such as 640, and the results will be different:

Figure 8. Ideal Active Pixels Formula

$$\begin{aligned}\text{NTSC: HSCALE} &= [(754 / \text{HACTIVE}) - 1] * 4096 \\ \text{PAL/SECAM: HSCALE} &= [(922 / \text{HACTIVE}) - 1] * 4096\end{aligned}$$

This is due to the fact that the actual active period is 646 pixels, not 640 pixels.

The first formula is commonly used when re-encoding, such as with set top box applications.

The second formula will be most convenient when attempting to fit the active image to a given window size.

The HSCALE values for a number of popular formats are provided in Table 1, which uses the formulas from Figure 7.

HDELAY

Once the scaling is determined, the third step is to figure the HDELAY register value, which can be calculated as follows in Figure 9:

Figure 9. Generic HDELAY Formula

$$\text{HDELAY} = \text{CLKX1_Horizontal_Delay} * \text{Scaling_Ratio}$$

$$\text{NTSC HDELAY} = 135 * (\text{HACTIVE} / 754) \& 0x3FE$$

$$\text{PAL HDELAY} = 186 * (\text{HACTIVE} / 922) \& 0x3FE$$

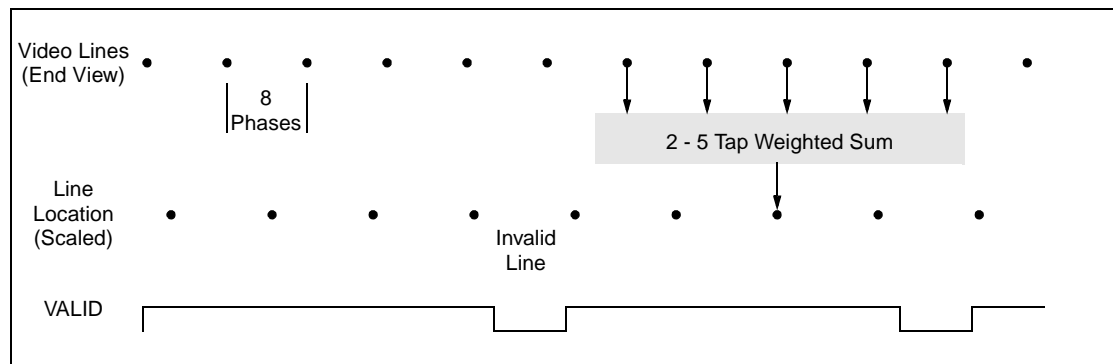
Use of Horizontal Registers for Horizontal Cropping

To horizontally crop an image, the values of HDELAY and HACTIVE are adjusted. To maintain proper image location, the cropped values of HDELAY and HACTIVE should be less than or equal to the value of HDELAY and HACTIVE without cropping. To crop the left side of an image, increase HDELAY by the number of pixels desired. To crop the right side of the image, decrease HACTIVE by the number of pixels desired. To fill a window, without adjusting window size, it may be necessary to rescale the image (which will affect HDELAY).

Vertical Scaling and Cropping

The generalized vertical scaling algorithm is depicted in Figure 10. The vertical scaling algorithm is similar to the horizontal scaling algorithm without the adjustments for sync detection and line length.

Figure 10. Vertical Scaling



Vertical Interpolation

The interpolation algorithm compares the available video lines and the desired, scaled vertical lines. The VSCALE register sets the scaler to the desired vertical line period.

The algorithm uses polyphase interpolation to generate the scaled lines from the available video lines. The desired sampled line location is determined to within 1/8 of a video line. The values between 1 and 8 are used to determine the coefficients used by the 2-tap weighted sum interpolator to calculate the output line. This is what gives Rockwell decoders the clear sharp images.

The decoder implements this scaling by using a single line store. Reducing the number of active pixels per line by horizontal downscaling can increase the number of taps in the vertical filter. Smaller line lengths allow storing multiple lines in the single line store. The decoder can implement up to a 5-tap interpolator.

For chroma data, the output lines are optionally comb filtered, and then decimated without interpolation filtering. This can be done due to the reduced chroma bandwidth to begin with.

Invalid Lines

Since the total number of input video lines may be greater than the desired number of scaled lines, there are times when there are two input video lines that produce a single expected scaled video line. This extra line period needs to be ignored, and is identified as an invalid line period.

Vertical Scaling Registers

VDELAY

Vertical scaling is achieved slightly differently than horizontal scaling. The most important difference is that vertical scaling (VSCALE) does not alter the vertical delay (VDELAY). This is important! As you may recall from the previous section, horizontal scaling does affect horizontal delay.

Valid video data does not start until line 21 for NTSC.

The default value for vertical delay (VDELAY) is 22. The units of VDELAY are half lines, while the units of VACTIVE are whole lines. VDELAY is the number half lines after the trailing edge of VRESET (i.e., after first nine lines for NTSC, which contain equalization and serration pulses. See Figure 11).

The falling edge of VACTIVE* indicates the beginning of the active video lines in a field. If VDELAY is even, the falling edge of VACTIVE* occurs $VDELAY / 2$ lines after the rising edge of VRESET* in the odd fields (1,3,5,7) and $(VDELAY / 2 + 1) / 2$ lines after the rising edge of VRESET* in the even fields (2,4,6,8).

Thus, if VDELAY is even, the first line of active video in the odd fields (1,3,5,7) will become the first line of a deinterlaced captured frame, and the first line of active video in the even fields (2,4,6,8) will become the second line of a deinterlaced captured frame. Likewise, if VDELAY is odd, the first line of active video in the odd fields (1,3,5,7) will become the second line of a deinterlaced captured frame, and the first line of active video in the even fields (2,4,6,8) will become the first line of a deinterlaced captured frame.

VACTIVE

When setting vertical scaling, the value for VACTIVE remains the same as for full resolution. Only VSCALE changes. The nominal value for NTSC vertical active (VACTIVE) is 480 lines. VACTIVE is only modified when cropping, which is discussed in a later section.

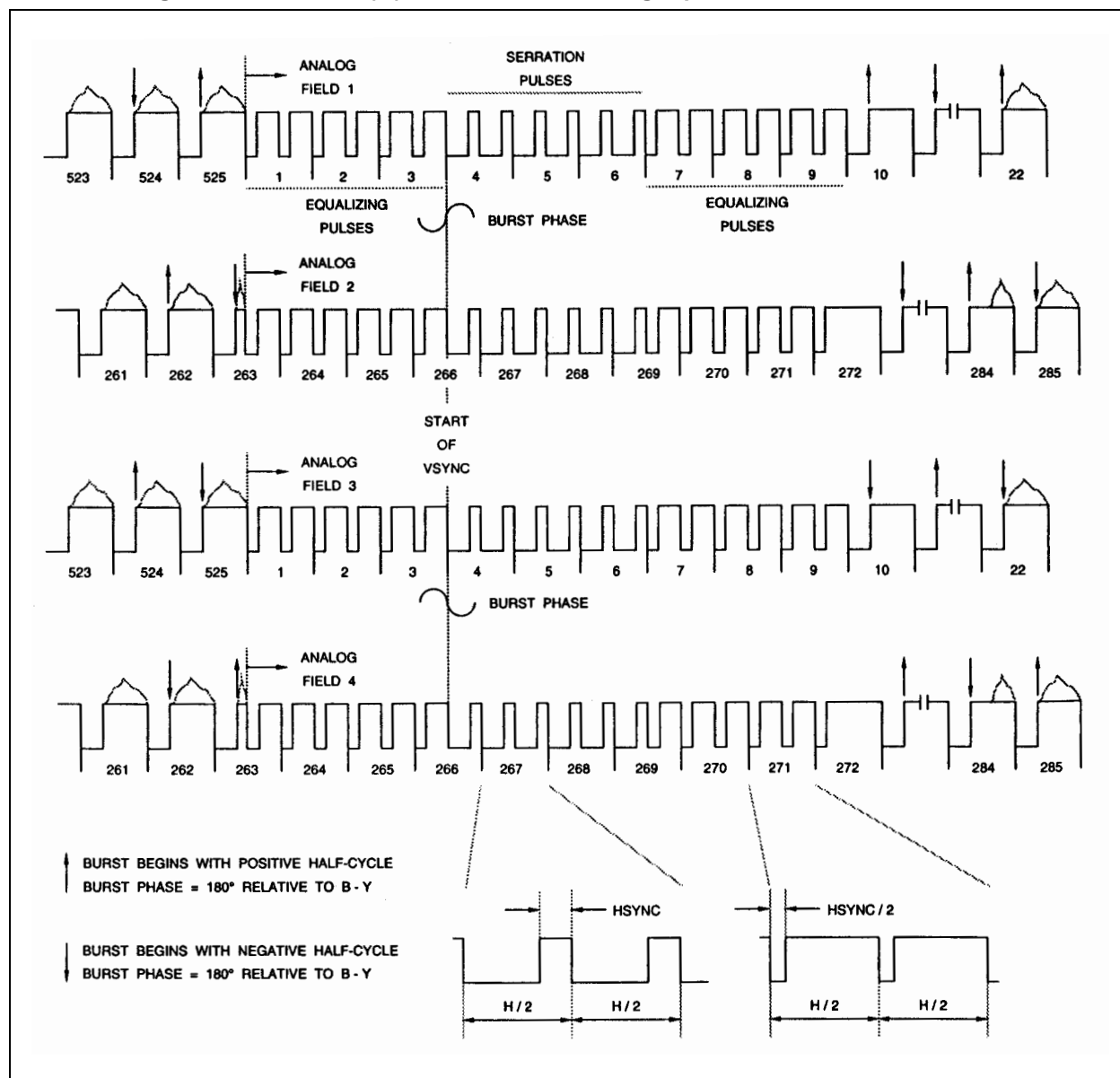
VSCALE

Vertical downscaling is easily achieved by using the following formula to calculate the value for the VSCALE register.

$$VSCALE = (0x1000 - \{[(scaling_ratio) - 1] * 512\}) \& 0x1FFF$$

Table 1 provides the VSCALE values for a number of popular formats. The table shows scaling values for two fields (interlaced), or single field (non-interlaced) applications. The recommendation for all formats of CIF scale and below, is to use single field scaling, for better display quality. Interlaced fields are required for any scaling from 2:1 to 1:1 resolution.

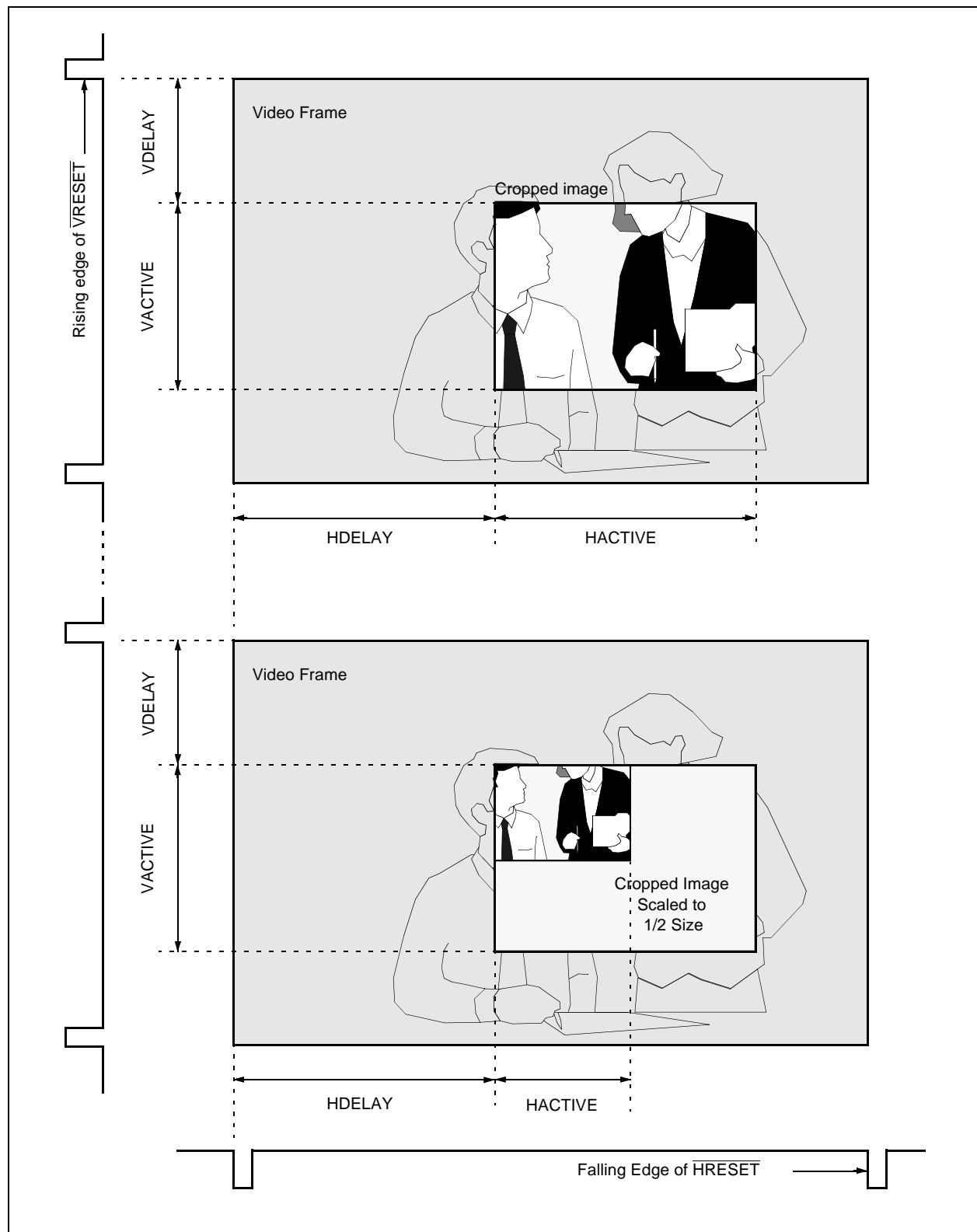
Figure 11 illustrates a four-field (M) NTSC format with equalization and serration pulses.

*Vertical Scaling and Cropping***Figure 11. Four-field (M) NTSC Format Showing Equalization and Serration Pulses****Use of Vertical Registers for Vertical Cropping**

To vertically crop an image, the values of VACTIVE and VDELAY are adjusted. To maintain proper image location, the cropped value of VACTIVE plus (VDELAY/2) should be less than or equal to the value without cropping (refer to Figure 12).

To crop the top of the image, increase VDELAY by the number of desired lines multiplied by two. To crop the bottom of the image, decrease VACTIVE by the number of desired lines. When the image is vertically scaled, then multiply the number of scaled lines to crop by the scale factor in order to get the number of full video lines to crop.

Figure 12. Effect of the Cropping and Active Registers



Output Interfaces

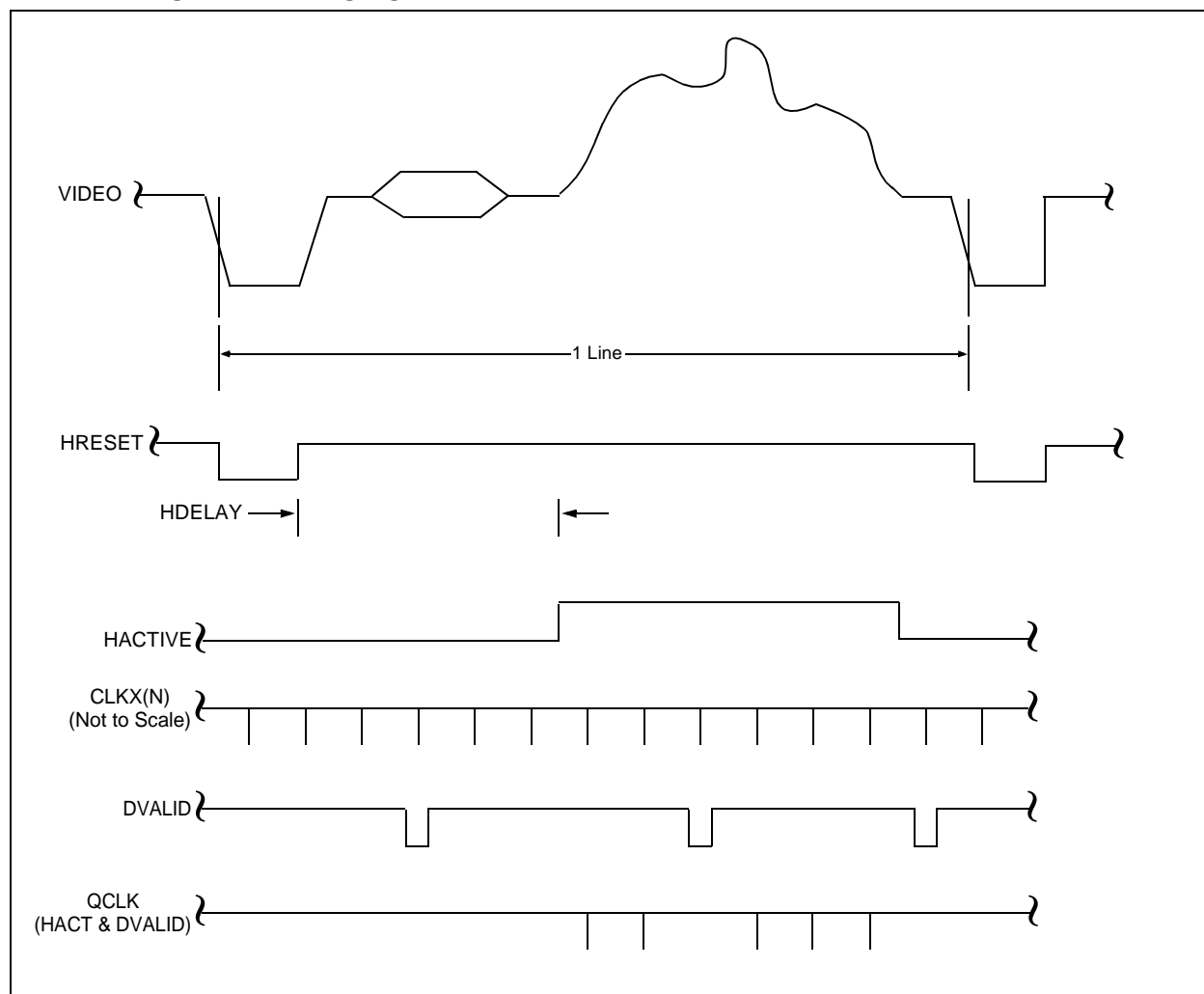
Horizontal Scaling and Cropping Effects

All Rockwell decoders have the following horizontal timing signals:

1. HACTIVE (or ACTIVE)
2. DVALID
3. CLKx1 (16 bit mode), CLKx2 (8 bit mode)
4. QCLK
5. HRESET
6. CBFLAG

The effects of scaling and cropping on each of these signals is described below (refer to Figure 13):

1. HACTIVE—This signal is used to determine when the analog active video is valid. Since horizontal video is always scaled, HACTIVE period will contain more clock transitions than the value programmed into the HACTIVE register, producing some invalid pixels. This signal is affected by the value programmed into the scaling register. Use DVALID to distinguish between valid and invalid pixels. When image cropping is taking place, the length of HACTIVE will be adjusted to provide fewer valid pixels per line.
2. DVALID—To determine which clocks are valid for storage into a video buffer the DVALID signal is high for valid pixels and low for invalid pixels. The DVALID toggles throughout the entire line time to include blanking and synchronizing intervals even with cropping. This signal is affected by the value programmed into the scaling register.
3. CLKx1—Input crystal frequency divided by 2. Except for Bt835, always a fixed frequency without any variation.
4. CLKx2—Input crystal frequency. (Except for Bt835), always a fixed frequency without any variation.
5. QCLK—this is generated using the equation $QCLK = HACTIVE \& DVALID \& CLKxN$. This signal provides a clock for every valid pixel only during the active period. This signal is ideal for a write pulse for memory or other interface devices. In addition, the gated signals can be programmed to be any combination of the three signals, or just the inverted form of CLKxN, by itself.
6. HRESET—occurs at the beginning of each line, not affected by horizontal scaling.
7. CBFLAG—informs the user whether the pixel is Cb or Cr. When invalid pixels are encountered the Cr, Cb order is maintained from valid pixel to valid pixel, as flagged by this signal pin. This signal is affected by the value programmed into the scaling register.

Figure 13. Timing Signals

Vertical Scaling and Cropping Effects

All Rockwell decoders have the following vertical timing interface signals:

1. VACTIVE (or ACTIVE)
2. FIELD
3. VRESET

The effects of scaling and cropping on each of these signals is described below:

1. VACTIVE—This signal is used to determine when the analog active video is valid. When vertical scaling occurs, VACTIVE is not affected, but the HACTIVE signal goes to its inactive state for the lines that should not be stored into the video memory. When image cropping is taking place, the length of VACTIVE will be adjusted to provide fewer lines per field.
In some video decoders, only the ACTIVE signal is available. This signal is the logical combination of HACTIVE and VACTIVE.
2. FIELD—Not affected by scaling or cropping.
3. VRESET—Not affected by scaling or cropping.

Conclusion

Scaling and cropping are two features of our decoders that are widely used by application programmers and need to be understood by hardware designers so the data is properly provided to the interfacing device. The information in this application note and the detailed descriptions in the decoder datasheet should provide sufficient information to fully comprehend the operation of these features. If you have further technical questions regarding this application note, please contact your local Rockwell FAE or call 800.854.8099 or 714.221.6996.



Web:
www.rss.rockwell.com

Email:
literature@rss.rockwell.com

For more information:
Call 1-800-854-8099

International Information:
Call 1-949-221-6996

**WORLDWIDE
HEADQUARTERS**
**Rockwell Semiconductor
Systems Inc.**

4311 Jamboree Road
P.o. Box C
Newport Beach, CA
92658-8902
Phone: (949) 221-4600
Fax: (949) 221-6375

**US Northwest/Pacific
Northwest**
Phone: (408) 249-9696
Fax: (408) 249-7113

**US Southwest
(Los Angeles)**
Phone: (805) 376-0559
Fax: (805) 376-8180

**US Southwest
(San Diego)**
Phone: (619) 535-3374
Fax: (619) 452-1249

**US Southwest
(Orange County)**
Phone: (949) 222-9119
Fax: (949) 222-0620

US North Central
Phone: (630) 773-3454
Fax: (630) 773-3907

US South Central
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Fax: (972) 407-0639

**Strategic Sales - Compaq
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Phone: (281) 376-5600
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Fax: (770) 246-0018

**US Southeast
(Raleigh, NC)**
Phone: (919) 786-4002
Fax: (919) 782-8727

US Florida/South America
Phone: (727) 799-8406
Fax: (727) 799-8306

US Mid-Atlantic
Phone: (215) 244-6784
Fax: (215) 244-9292

Brazil
Phone: (55-11) 3874 8978
Fax: (55-11) 3874 8883

European Headquarters
Rockwell Semiconductor
Systems S.A.S.
Les Taissounieres B1
1680 Route des Dolines
BP 283
06905 Sophia Antipolis Cedex,
France
Phone: (33) 4 93 00 33 35
Fax: (33) 4 93 00 33 03

Europe Central
Phone: (49-89) 829-1320
Fax: (49-89) 834-2734

Europe Mediterranean
Phone: (39 02) 93179911
Fax: (39 02) 93179913

**Europe Mediteranean
(Satellite)**
Rockwell Semiconductor
Systems
c/o Rockwell Automation S.r.l.
Belmonta de Tajò, 31
Phone: (34) 91 565 16 16
Fax: (34) 91 565 16 87

Israel
Phone: (972-9) 9524 000
Fax: (972-9) 9573 732

Europe North
Phone: (44-1344) 486 444
Fax: (44-1344) 486 555

**Europe North
(Satellite)**
Phone: (46) 8 477 4036
Fax: (46) 8 477 4037

Europe South
Phone: (33-1) 49 06 39 80
Fax: (33-1) 49 06 39 90

APAC Headquarters
Rockwell International
ManufacturingPte. Ltd.
1 Kim Seng Promenade
#09-01 East Tower
Great World City
Singapore 237994
Phone: (65) 737 7355
Fax: (65) 737 9077

Australia
Phone: (61-2) 9869 4088
Fax: (61-2) 9869 4077

China/Beijing
Phone: (86-10) 6518-2545
Fax: (86-10) 6518-2536

China/Shanghai
Phone: (86-21) 6361 2515
Fax: (86-21) 6361 2516

Hong Kong
Phone: (852) 2827 0181
Fax: (852) 2827 6488

India
Phone: (91-11) 6924 780
Fax: (91-11) 6924 712

Korea
Phone: (82-2) 565 2880
Fax: (82-2) 565 1440

Taiwan Headquarters
Rockwell International,
Taiwan Company Limited
Room 2808
International Trade Building
333, Keelung Road, Section 1
Taipei, Taiwan, 10547 ROC
Phone: (886-2) 2720 0282
Fax: (886-2) 2757 6760

Japan Headquarters
Rockwell International
Japan company Limited
Shimomoto Building
1-46-3 Hatsudai, Shibuya-ku
Tokyo, 151 Japan
Phone: (81-3) 5371 1520
Fax: (81-3) 5371 1501

Document Number:

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